Đồ án 2: DESIGN AND SIMULATION I2C PROTOCOL BY VERILOG

Thời gian: Tuần 9

Nội dung: Test plan + Code RTL 45% chức năng

**Test plan**

|  |  |  |
| --- | --- | --- |
| TT | Thời gian | Nội Dung |
| 1 | 21/10 - 27/10 | Test case Master |
| 2 | 28/10 - 3/11 | Test case Slave |
| 3 | 4/12 - 10/12 | Test I2C protocol + CLK DIV |

**Diagram**

